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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/620,468 | 07/15/2003 | Dinesh Chopra | MI22-2345 | 8630 |

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| EXAMINER | |
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| **ART UNIT** | **PAPER NUMBER** |
| 2822 | |

DATE MAILED: 02/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/620,468 | DINESH CHOPRA | |
| | Examiner | Art Unit | |
| | Thanh Y. Tran | 2822 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *17 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *55-68* is/are pending in the application.

4a) Of the above claim(s) *1-54 and 69-78* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *55-68* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/15/03 & 12/17/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 55-56 and 58-61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al (U.S. 6,100,195) in view of Hem P. Takiar (UK 2184288).

As to claim 55, Chan et al discloses in Figs. 2D-2H a conductive connection forming method comprising: forming a first layer (56) comprising copper ("interconnect copper line") over a substrate (52) (see col. 4, lines 31-37), forming a second layer (59) comprising a second metal different from copper over the first layer, the second metal comprising palladium (see col. 4, lines 43-49), incorporating at least some of the palladium into an intermetallic layer (61) comprising the palladium and copper (see 4, lines 49-55, layer 61 comprising palladium and copper), removing at least a portion of any second metal (59) (see figures 2F-2G) that is not incorporated into the intermetallic layer (61) and exposing the intermetallic layer (61) (see Fig. 2G), and forming a conductive connection (see Fig. 2J) directly to the intermetallic layer (61) without a passivation layer therebetween.

Chan et al does teach the intermetallic layer (palladium-copper layer) having a thickness of from about 50 to about 150 Angstroms.

Hem P. Takiar teaches in figure 7, the layer having a thickness of from about 50 to about 150 Angstroms ("80-300 Angstroms") (see the ABSTRACT in Hem P. Takiar). Therefore, it

would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the conductive connection forming method of Chan et al by using the layer having a thickness of from about 50 to about 150 Angstroms ("80-300 Angstroms") as taught by Hem P. Takiar for providing a suitable use since palladium has a very low diffusivity into copper (see the ABSTRACT in Hem P. Takiar).

As to claim 56, Chan et al discloses in Figs. 2D-2H a conductive connection forming method, wherein the intermetallic layer (61) consists of copper and palladium (see 4, lines 49-55, layer 61 comprising palladium and copper).

As to claim 58, Chan et al discloses in Figs. 2D-2H a conductive connection forming method, wherein the first layer (56) has an elevational thickness-before the incorporating, further comprising removing any second metal (59, see figure 2F-2G) not comprised by the intermetallic layer (61), and any portion of the intermetallic layer (61), beyond the elevational thickness.

As to claim 59, Chan et al discloses in Figs. 2D-2H a conductive connection forming method, wherein the removing comprises chemical mechanical polishing (see col. 3, line 65 – col. 4, line 8; and col. 4, lines 38-42).

As to claim 60, Chan et al discloses in Figs. 2D-2H a conductive connection forming method, wherein a rate of removing the second layer (59) compared to the intermetallic material (material of element 61) inherently comprises greater than 5 to 1 (it should be noted that: the rate of removing the second layer 59 compared to the intermetallic material (material of element 61) is inherently comprises greater than 5 to 1 because the materials for the second layer 59 and intermettallic layer 61 in the reference of Chan et al are the same materials as disclosed in the present invention, thus they must inherently have the same rate (greater than 5 to 1).

As to claim 61, Chan et al discloses in Figs. 2D-2H a conductive connection forming method, wherein the second layer (59) consists of palladium (see col. 4, lines 43-49).

3. Claim 57 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al (U.S. 6,100,195) in view of Hem P. Takiar (UK 2184288) as applied to claim 55 above, and further in view of McTeer (U.S. 6,069,075).

As to claim 57, Chan et al in view of Hem P. Takiar does not teach the incorporating comprises annealing the first and second layer at a temperature of greater than 400 to about 500 °C. McTeer (U.S. 6,069,075) teaches the process of annealing the layers at a temperature of greater than 400 to about 500°C ("440 to 480 degree C") (see col. 3, line 60 – col. 4, line 5). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method of Chan et al in view of Hem P. Takiar by applying a temperature of greater than 400 to about 500 °C ("440 to 480 degree C") as taught by McTeer for reducing reflectance or forming a desired anti-reflective coating (see col. 3, line 60 – col. 4, line 5 in McTeer).

4. Claims 62-63 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al (U.S. 6,100,195) in view of McTeer (U.S. 6,069,075) and Hem P. Takiar (UK 2184288).

As to claim 62, Chan et al discloses in Figs. 2D-2H an oxidation protection method for metal-containing material during semiconductor processing, comprising: forming a first metal-containing material (56) over a substrate (52), forming a second metal-containing material (59) over the first metal-containing material (56), annealing the first and second metal-containing

materials (56, 59) to form an intermetal material (61) from some of the first material (56) and at least some of the second material (59); and after the annealing, exposing the intermetal material (61, see figure 2G) to conditions effective to oxidize the first metal-containing material (56) but the intermetal material (61) protecting at least some of the first metal-containing material (56) from oxidation during the exposing.

Chan et al does not teach annealing the first and second metal-containing materials at a temperature of greater than 400 to about 500 °C; and the intermetal material having a thickness of from about 50 to about 150 Angstroms.

McTeer (U.S. 6,069,075) teaches the process of annealing the layers at a temperature of greater than 400 to about 500°C ("440 to 480 degree C") (see col. 3, line 60 – col. 4, line 5). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method of Chan et al by applying a temperature of greater than 400 to about 500 °C ("440 to 480 degree C") for annealing the layers as taught by McTeer for reducing reflectance or forming a desired anti-reflective coating (see col. 3, line 60 – col. 4, line 5 in McTeer).

Hem P. Takiar teaches in figure 7, the layer having a thickness of from about 50 to about 150 Angstroms ("80-300 Angstroms") (see the ABSTRACT in Hem P. Takiar). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the conductive connection forming method of Chan et al by using the layer having a thickness of from about 50 to about 150 Angstroms ("80-300 Angstroms") as taught by Hem P. Takiar for providing a suitable use since palladium has a very low diffusivity into copper (see the ABSTRACT in Hem P. Takiar).

As to claim 63, Chan et al discloses in Figs. 2D-2H an oxidation protection method for metal-containing material during semiconductor processing, wherein the first metal-containing material (56) consists essentially of copper (see col. 4, lines 31-37), and the intermetal material (61) consists of copper and palladium (see 4, lines 49-55, layer 61 comprising palladium and copper).

5. Claims 64-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al (U.S. 6,100,195) in view of McTeer (U.S. 6,069,075)

As to claim 64, Chan et al discloses in Figs. 2D-2H an oxidation protection method for metal-containing material during semiconductor processing, comprising: forming a first level of integrated circuit wiring (layer 56 comprising a first level of integrated circuit wiring) over a semiconductive substrate (52), the first wiring level comprising copper (layer 56 comprising the first wiring level and comprising copper, see see col. 4, lines 31-37), forming an intermetallic material (61) at least partially within the first wiring level, the intermetallic material (61) comprising copper and palladium (see 4, lines 49-55, layer 61 comprising palladium and copper), and forming a conductive via ("hole 65") (see figure 2I) on and in electrical contact with the intermetallic material (61).

Chan does not teach forming an intermetallic material at a temperature of greater than 400 to about 500 °C.

McTeer (U.S. 6,069,075) teaches the process of forming a layer at a temperature of greater than 400 to about 500°C ("440 to 480 degree C") (see col. 3, line 60 – col. 4, line 5). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the

invention was made to modify the method of Chan et al by applying a temperature of greater than 400 to about 500 °C ("440 to 480 degree C") for a forming a layer as taught by McTeer for reducing reflectance or forming a desired anti-reflective coating (see col. 3, line 60 – col. 4, line 5 in McTeer).

As to claim 65, Chan et al discloses in Figs. 2D-2H an oxidation protection method for metal-containing material during semiconductor processing, wherein the forming the intermetallic material (61) comprises: forming a layer comprising the palladium (layer 59 comprising palladium) on the first wiring level (first wiring level of first-level layer 56); annealing the layer (59) and first wiring level (first wiring level of first-level layer 56); and removing at least some of any palladium (59) not comprised by the intermetallic material (61) and leaving a sufficient thickness of intermetallic material (61) to reduce oxidation of the first wiring level where the via ("hole 65") (see figure 2I) connects to the first wiring level.

As to claim 66, Chan et al discloses in Figs. 2D-2H an oxidation protection method for metal-containing material during semiconductor processing, wherein the forming the via ("hole 65") (see figure 2I) further comprises forming a second level of integrated circuit wiring (second level of integrated circuit wiring of layer 59) over the first wiring level (first wiring level of layer 56) during formation of the conductive via ("hole 65") (see figure 2I).

As to claim 67, Chan et al discloses in Figs. 2D-2H an oxidation protection method for metal-containing material during semiconductor processing, wherein the first level (first layer of layer 56) consists of copper (see col. 4, lines 31-37).

As to claim 68, Chan et al discloses in Figs. 2D-2H an oxidation protection method for metal-containing material during semiconductor processing, wherein the intermetallic material

(61) consists of copper and palladium (see 4, lines 49-55, layer 61 comprising palladium and copper).

***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Obeng et al (U.S. 6,323,131) discloses passivated copper surfaces.

Dunbin et al (U.S. 5,891,513) discloses electroless CU deposition on a barrier layer by CU contact displacement for ULSI applications.

Rodbell et al (U.S. 5,071,714) discloses multilayered intermetallic connections for semiconductor devices.

Restaino et al (U.S. 6,140,236) discloses high throughput A1-CU thin film sputtering process on small contact via for manufacturable BEOL wiring.

Tobben et al (U.S. 6,261,950) discloses self-aligned metal caps for interlevel metal connections.

***Contact Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (571) 272-2110. The examiner can normally be reached on M-F (9-6:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TYT

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